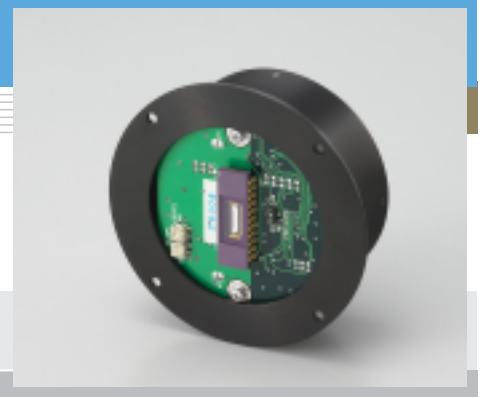


# NMOS multichannel detector head C8892

Integrated low-noise driver/amplifier circuit for NMOS linear image sensor



C8892 is multichannel detector head incorporating low-noise driver/amplifier circuit developed for Hamamatsu NMOS linear image sensors. C8892 is designed especially for compactness, having an overall length as short as 40 mm or less. In addition, C8892 is designed for ease of use. It is provided with circular flange for connection to monochromator and adjustment mechanism for optical alignment for NMOS linear image sensor. The flange is interchangeable, thus facilitating connection to various models of monochromator. The housing case also provides a shielding effect against external noise. As useful options, peripheral devices are available for driving C8892, and for the output signal processing.

### Features

- Low noise
- Wide dynamic range
- Operatable with simple input signals  
(Only a master start pulse, a master clock pulse,  $\pm 15$  V are required.)
- Interchangeable flange
- Simple electrical and optical adjustments

### Applications

- Multichannel spectrophotometry
- Optical spectrum analysis
- Time-resolved photometry

#### ■ Compatible NMOS linear image sensors

Type No. of NMOS linear image sensor *1	Number of pixels	Active area per pixel (pixel pitch × height)
S3901-128Q, S8380-128Q	128	50 $\mu$ m × 2.5 mm
S3901-256Q/F, S8380-256Q	256	
S3901-512Q/F, S8380-512Q	512	
S3902-128Q	128	50 $\mu$ m × 0.5 mm
S3902-256Q/F	256	
S3902-512Q/F	512	
S3903-256Q	256	25 $\mu$ m × 0.5 mm
S3903-512Q/F	512	
S3903-1024Q/F	1024	
S3904-256Q, S8381-256Q	256	25 $\mu$ m × 2.5 mm
S3904-512Q/F, S8381-512Q	512	
S3904-1024Q/F, S8381-1024Q	1024	

\*1: The suffix of type number indicates:  
Q: quartz window, F: fiber optic window

■ Absolute maximum ratings

Parameter	Symbol	Value	Unit
Supply voltage (analog)	Va	±18	V
Operating temperature	Topr	0 to 50 *2	°C
Storage temperature	Tstg	-10 to 60 *2	°C

\*2: No condensation

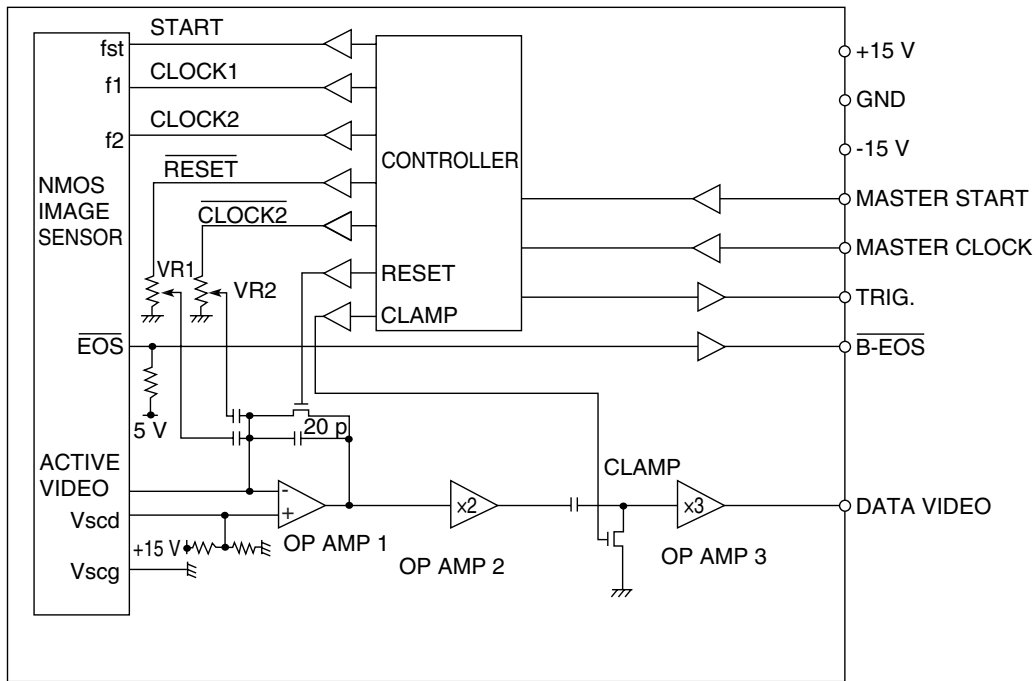
■ Electrical characteristics (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	
Input	Supply voltage	Analog	Va	±14.5	±15.0	±15.5	V
	Master start pulse (φms)	Voltage	Vms (H)	2.0	5.0	-	V
			Vms (L)	0	-	0.8	
		Width	tpwφms	1/fφmc	-	-	s
	Rise/fall Time	trφms, tfφms	-	-	500	ns	
	Master clock pulse (φmc)	Voltage	Vmc (H)	2.0	5.0	-	V
			Vmc (L)	0	-	0.8	
		Frequency	fφmc	-	-	375	kHz
		Width *3	tpwφmc	30	-	-	ns
	Rise/fall time	trφmc, tfφmc	-	-	500	ns	
Output *4	Start pulse (φst)	Voltage	Vst (H)	4.75	5.0	-	V
			Vst (L)	0	-	0.4	
		Rise/fall time	trφst, tfφst	-	-	100	ns
	Width	tpwφst	-	2/fφmc	-	s	
	Clock pulse (φ1, φ2)	Voltage	V1, V2 (H)	4.75	5.0	-	V
			V1, V2 (L)	0	-	0.4	
	Rise/fall time	trφ1, trφ2	-	-	100	ns	
	tfφ1, tfφ2	-	-	-			
	Clock pulse (φ1) width		tpwφ1	-	3/fφmc	-	s
	Clock pulse (φ2) width		tpwφ2	-	3/fφmc	-	s
End of scan pulse	Voltage	Veos (H)	4.75	5.0	-	V	
		Veos (L)	-	-	0.4		
	Rise/fall time	treos, tfeos	-	-	100	ns	
Width		tpweos	-	3/fφmc	-	s	
Trigger pulse	Voltage	Vtrig (H)	4.0	5.0	-	V	
		Vtrig (L)	0	-	0.4		
Rise/fall time		trtrig, tftrig	-	-	100	ns	

\*3: The operation of 50 % Typ. duty ratio is recommended.

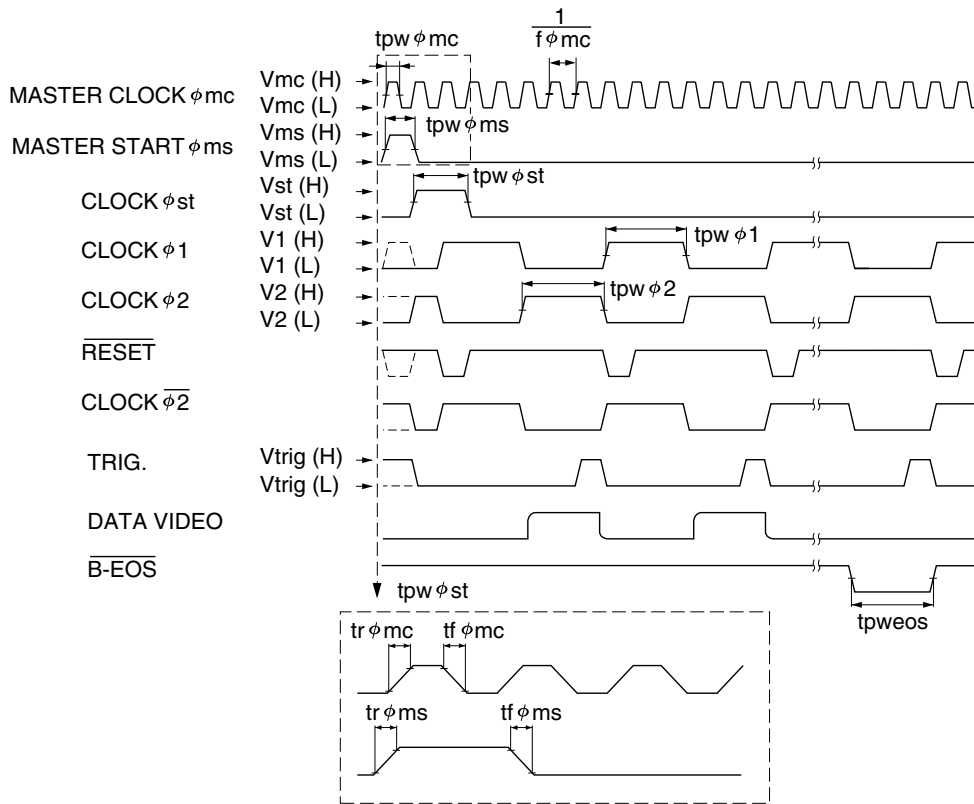
\*4: The outputs of start-pulse and clock-pulse are to be obtained from a front part where an image sensor is installed. The outputs of end-of-scan and trigger-pulse are to be obtained from a back-side part where a connector for input/output signal is fixed.

■ Block diagram



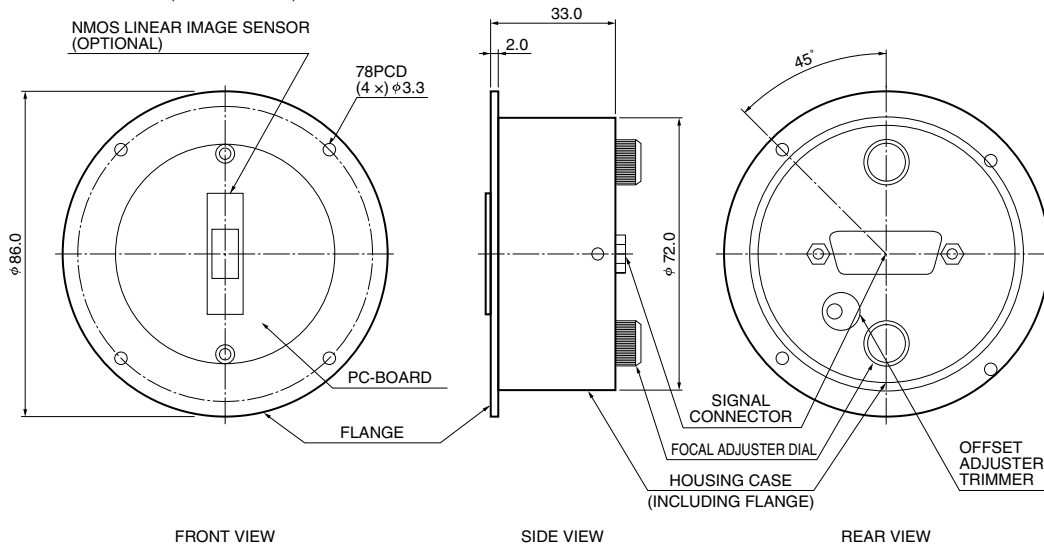
KACCC0171EA

■ Timing chart



KACCC0172EA

■ Dimensional outline (unit: mm)

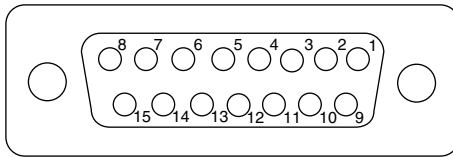


The focal position can be adjusted backward within the range from 0 to 4.5 mm (circuit stroke length) with a focal adjustment dial.

WEIGHT: approx. 0.16 kg

KACCA0113EA

■ Pin assignment of "Signal I/O" connector (15-pin D-sub socket type)



KACCC0069EA

Terminal No.	Terminal name	Description
1	NC	No connection
2	Data video	Analog video signal output; positive polarity
3	+15 V	Positive power supply (25 mA)
4	-15 V	Negative power supply (15 mA)
5	NC	No connection
6	Start	Digital input signal for initializing the circuit; positive logic. Interval of these pulses equals the integration time of the sensor
7	CLK	Digital input signal for operating the circuit at the rising edge
8	EOS	Digital output signal indicating end of scan, negative logic
9	A. GND	Analog ground
10	A. GND	Analog ground
11	Shield	Case shield
12	D. GND	Digital ground
13	D. GND	Digital ground
14	D. GND	Digital ground
15	Trigger	Digital output signal for A/D conversion; positive logic

- Video data rate is 1/6 of master clock frequency (62.5 kHz Max.).
- The operation of circuit stroke length below 4.5 mm is recommended.
- The relation between data video output voltage and output charges from NMOS image sensor can be expressed by the following formula.

$$V_{out} (V) = 3 \times \frac{\text{Output charge}}{10 \times 10^{-12}[F]}$$

Note) Amplifier saturation voltage is 10 V.

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